

ANNA UNIVERSITY :: CHENNAI – 600 025

MODEL QUESTION PAPER

VI - SEMESTER

B.E. ELECTRICAL AND ELECTRONICS ENGINEERING

EE340 - MICRO PROCESSOR AND APPLICATIONS

Time: 3hrs.

Max Marks: 100

Answer all Questions

PART – A (10 x 2 = 20 Marks)

1. Distinguish between **wait state and bus idle** condition.
2. What is the need for **timing diagram**?
3. What is the function of queue in 8086 microprocessor?
4. What is the advantage of using an **internal register** for temporary data storage over the memory location?
5. What are the **features of 8051** micro controller?
6. What is the function of watch dog timer in 8096 micro controller?
7. Mention the advantage of **memory mapped I/O**.
8. What is meant by multiplexed scanned seven segment LED display interfacing?
9. What is the need for **8254 programmable interval timer** and mention its applications?
10. What are the functions performed by the **Intel 8251 USART**?

PART – B (5 x 16 = 80 Marks)

11. Draw the **functional block diagram 8031 microcontroller** and explain the function of each block. (16)
- 12.a)i) Draw the **organization of a 8085 based micro computer system** and explain. (10)
ii) Explain the various **addressing modes in 8085 processor**. (6)

OR

- 12.b)i) Draw and discuss the **timing diagram for memory read operation of 8085** processor. (8)
- ii) Explain the different techniques used for **interfacing I/O devices with 8085 processor**. State the merits and demerits of each. (8)
- 13.a)i) How is pipelined architecture implemented in 8086 processor? (10)
- ii) Draw and explain the memory structure of 8086 processor. (6)

OR

- 13.b) Draw the complete schematic of 8086 processor memory interface in minimum mode with the following specification.
- i. 16K of EPROM
 - ii. 32K of RAM. Also indicate the address map. (Use separate chip for odd and even memory) (16)
- 14.a)i) Design a seven segment LED output port with device address F5 H, using a 74LS138 3-to-8 decoder, a 74LS20 4 input NAND gate, a 74LS02 NOR gate and a common anode seven segment LED. (10)
- ii) Compare **memory mapped I/O and I/O mapped I/O structure**. (6)

OR

- 14.b) Interface **DAC 0808 with 8085, use 8255 PPI** as a parallel port to send digital data to DAC. Write a program to generate square wave using the above hardware. (16)
- 15.a)i) What are the over heads associated with interrupt driven input-output and how are they reached using **DMA**? (4)
- ii) Explain the operation of **8257 direct memory access controller** with its functional block diagram. (12)

OR

- 15.b) Explain the need and the features of the following ICs: (16)
- (i) The Intel **8259 – Programmable Interrupt Controller**. (ii) The Intel **8279 – Key board/ Display controller**.