

ANNA UNIVERSITY :: CHENNAI – 600 025

**MODEL QUESTION PAPER
V SEMESTER**

B.E. ELECTRONICS AND COMMUNICATION ENGINEERING

EC336 – COMPUTER ARCHITECTURE

Time: 3hrs

Max Marks: 100

Answer all Questions

PART – A (10 x 2 = 20 Marks)

1. What are the three ways to represent a negative number and give an example for each one.
2. Why do we need biased exponent representation in floating point numbers?
3. Write Booth's expression for a signed binary number, 110101
4. Construct a four-segment floating-point adder pipeline and specify the operation to be performed in each segment.
5. Compute the number of clock pulse needed to process 100 tasks in a eight segment pipeline.
6. A processor has a microinstruction format containing 8 separate control fields C₀:C₇. Each C_i can activate any one of N_i (i varies from 1 to 8) distinct control lines, where N₁ = 5, N₂ = 3, N₃= 9, N₄=1, N₅=7, N₆=12, N₇=2, N₈=3. What is the width of the control field (i) In case Vertical Microprogramming? (ii) in case of Horizontal Microprogramming.
7. What additional logic is required to give a no-match result for a word in an associative memory when all key bits are zero?
8. Compare and contrast LRU and LFU replacement policies.
9. What is PCI interrupts?
10. Write any two Communication methods.

PART – B (5 x 16 = 80 Marks)

11. With a neat diagram, explain the internal organization of a digital computer.
- 12.a) Draw the circuit diagram for 4 bit binary adder and subtractor and explain how this can be used to construct BCD Adder / Subtractor.

(OR)

- 12.b)i) Explain the Booth's Multiplication algorithm for binary numbers by considering 10101 and 101 as examples.
ii) Describe the modified Booth's algorithm for the same example.

- 13.a) Discuss the various methods of Microprogramming Sequencing Techniques with examples.

(OR)

- 13.b) Write Short notes on (i) Nano Programming and (ii) Super Scalar Processing

- 14.a) Explain the concept of Virtual memory with paging hardware and software. Consider the following case as example: A virtual memory and main memory address spaces are of sizes 8K and 4K respectively.

(OR)

- 14.b) Briefly explain the Set-Associative Mapping by considering a main memory of size 1MB and a Cache memory of size 4k. Compute the width of the cache memory, if a two-way set associative mapping is used. Assume the width of the data bus

- 15.a) Explain Direct Memory Access mode of data transfer with neat sketch.

(OR)

- 15.b) Briefly explain the interrupt initiated I/O and describe how the priority is assigned to the interfacing devices.
