D 248

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2003.

Fourth Semester

Electronics and Communication Engineering

EC 242 — DIGITAL ELECTRONICS

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. If A and B are boolean variables check if $(A \cdot \overline{A}) \oplus (A \oplus \overline{A}) = (B + \overline{B}) \oplus (\overline{B} \oplus B)$.

2. For a switching function of n variables, how many distinct min terms and max terms are possible?

3. An inverter circuit with N–channel MOSFETs works with ———— logic.

4. If a manufacturer specifies the minimum logical 1 at a gate output a 4.0 V and also specifies that any voltage down upto 3.6 V will be considered as logical 1, find the noise margin.

5. State the condition for $B = I_2$ in the Boolean expression $B = I_0 \overline{S_0}\, \overline{S_1} + I_1 \overline{S_0} S_1 + I_2\, S_0 \overline{S_1} + I_3 S_0 S_1$. What is the combinational logic circuit realised by the above boolean expression?

6. State the condition to check the equality of two n–bit binary numbers A and B.

7. What is the condition on the JK flip flop to work as a D flip flop?

8. Name two sequential switching circuits.

9. What is race–around condition?

10. What is the cause for essential hazard?

PART B — ($5 \times 16 = 80$ marks)

11. (i) Find a minimal sum–of–products representation for $f(A, B, C, D, E) = \sum m\ (1, 4, 6, 10, 20, 22, 24, 26) + d\ (0, 11, 16, 27)$ using Karnaugh map method. Draw the circuit of the minimal expression using only NAND gates. (11)

(ii) Prove that $(x_1 + x_2) \cdot (x_1' \cdot x_3' + x_3)(x_2' + x_1 x_3)' = x_1' x_2$. (5)

12. (a) (i) Explain the working of a basic totem–pole TTL two input NAND gate. (10)

(ii) Explain the terms : Fan in, Fan–out, Propagation–delay. (6)

Or

(b) Explain the working of :

(i) three input ECL NOR gate. (8)

(ii) two input CMOS NAND gate. (8)

13. (a) (i) Design a full adder and a full subtractor. (14)

(ii) Draw the block diagram of a 2's complement adder/subtractor. (2)

Or

(b) (i) Design and explain the working of a 1 to 8 demultiplexer. (10)

(ii) Write notes on : ROM, EPROM, PLA. (6)

14. (a) (i) Explain working of Master/Slave JK flip flop. (8)

(ii) Design and explain the working of an up–down ripple counter. (8)

Or

(b) Design and explain the working of a synchronous mod–3 counter. (16)

15. (a) (i) What is a fundamental mode sequential circuit? (2)

(ii) Define cycle. (2)

(iii) Write notes on Races and Hazards. (6 + 6)

Or

(b) Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0, the output does not change for any change in X. Use SR latch for implementation of the circuit. (16)

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